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REMARKS

Upon entry of this Response, claims 1-3, 7-18, and 19 remain pending in the present Patent Application. Claims 1, 9, 15, and 19 have been amended, and claims 4-6 and 17-18 have been canceled herein. Applicant requests reconsideration of the pending claims in view of the following remarks.

In item 2 of the Office Action, the Office Action requests a legible copy of a reference since a website could not be found. Accompanying this Response is a Supplemental Information Disclosure Statement and form 1449 with additional cited references including a copy of the reference in question.

Next, in items 3 and 4, claim 4 has been both objected to and rejected for the grounds noted. Claim 4 has been canceled herein, thereby rendering this grounds for rejection moot with respect to such claim.

Next, in item 5 of the Office Action, claims 1, 3, 7, 8, and 15 have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,301,623 issued to Simpson et al. (hereafter "Simpson"). Anticipation under §102 "requires the disclosure in a single prior art reference of each element of the claim under construction. W.L. Gore & Associates, Inc. v. Garlock, Inc., 220 USPQ 303, 313 (Fed. Cir. 1983). For the reasons that follow, Applicant requests that the rejection of claims 1, 3, 7, 8, and 15 be withdrawn.

To begin, claim 1 has been amended to recite as follows:

1. A serial bus expansion circuit, comprising:
a bus distribution circuit selectively coupling a serial bus to one of a number of serial bus outputs;
a distribution controller having a control output coupled to a control input of the bus distribution circuit; and
a number of power-up pull resistors coupling each of the serial bus outputs to a power-up pull source, the power-up pull source including a state circuit that sequentially places a switch in a first state coupling a source voltage to the power-up pull resistors and in a second state coupling a common voltage to the power-up pull resistors in response to a system power-up condition.

Claim 1 has been amended to incorporate the subject matter of claim 4 canceled herein. Also, claim 15 has been amended to incorporate the subject matter of claims 17 and 18 canceled herein. Applicant asserts that Simpson fails to show or suggest the elements of claims 1 and 15 as amended herein. In addition, the Office Action admits that Simpson fails to show or suggest the elements of claim 4 and 17 incorporated into claims 1 and 15. Accordingly, Applicant requests that the rejection

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of claims 1 and 15 be withdrawn. In addition, Applicant requests that the rejection of claims 3, 7, and 8 be withdrawn as depending from claim 1 as amended.

In item 6 of the Office Action, claims 2, 4-6, 9-14, and 16-19 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Simpson in view of the I2C Specification, version 2.1, January 2000 (hereafter "I2C Spec"). A prima facie case of obviousness is established only when the prior art teaches or suggests all of the elements of the claims. MPEP §2143.03, In re Rijckaert, 9 F.3d 1531, 28 U.S.P.Q2d 1955, 1956 (Fed. Cir. 1993). Applicant notes that claim 1 has been amended so as to incorporate the subject matter of claim 4 now canceled. Similarly, claim 15 has been amended herein to incorporate the subject matter of claim 17 and 18. Thus, the rejection of claims 4 and 17-18 is addressed herein with reference to claims 1 and 15 as amended. For the reasons that follow, Applicant asserts that the cited combination of Simpson and the I2C Spec fails to show or suggest each of the elements of claims 1, 2, 9-14, 16, and 19. Accordingly, Applicant requests that the rejection of claims 1, 2, 9-14, 16, and 19 be withdrawn. In addition, it is noted that claims 4-6 and 17-18 have been canceled herein, thereby rendering this grounds of rejection moot with respect to such claims.

To begin, claim 1 amended to incorporate the subject matter of claim 4 now canceled states as follows:

1. A serial bus expansion circuit, comprising:
a bus distribution circuit selectively coupling a serial bus to one of a number of serial bus outputs;
a distribution controller having a control output coupled to a control input of the bus distribution circuit; and
a number of power-up pull resistors coupling each of the serial bus outputs to a power-up pull source, the power-up pull source including a state circuit that sequentially places a switch in a first state coupling a source voltage to the power-up pull resistors and in a second state coupling a common voltage to the power-up pull resistors in response to a system power-up condition.

In this respect, the power-up pull resistors that couple each of the serial bus outputs to the power-up pull source are controlled by a state circuit that sequentially places a switch in a first state that couples the source voltage to the power-up pull resistors and in a second state that couples the common voltage to the power-up pull resistors in response to a system power-up condition. With respect to claim 4 now incorporated into claim 1 as amended, the Office Action states:

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"However, Simpson does not explicitly disclose the power-up pull source includes a state circuit that sequentially switches in a first state coupling a source voltage to the power-up pull resistors and in a second state coupling a common voltage to the power-up pull resistors in response to a system power-up condition. I2C Spec teaches a) includes a [sic] state circuit that sequentially switches in a first state coupling a source voltage to the power-up pull resistors and in a second state coupling a common voltage to the power-up pull resistors in response to a system power-up condition (e.g. START and STOP conditions) (note at least section 6.2 and table 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a state circuit that sequentially switches in a first state coupling a source voltage to the power-up pull resistors and in a second state coupling a common voltage to the power-up pull resistors in response to a system power-up condition as taught by I2C Spec in the system of Simpson to indicate a START condition." (Office Action, pages 5-6).

Applicant respectfully disagrees. Specifically, the I2C Spec does not teach transitioning the voltages applied to the power-up pull resistors from a source voltage to a common voltage based upon a system power-up condition. Rather, such transitions are taught by the I2C Spec for START and STOP conditions relating to the START and STOP of the transmission of data. Specifically, Section 6.2 of the I2C Spec states as follows:

6.2 START and STOP conditions

Within the procedure of the I²C-bus, unique situations arise which are defined as START (S) and STOP (P) conditions (see Fig. 5).

A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition. This bus free situation is specified in Section 15.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In this respect, the START (S) and repeated START (Sr) conditions are functionally identical (see Fig. 10). For the remainder of this document, therefore, the S symbol will be used as a generic term to represent both the START and the repeated START conditions, unless Sr is particularly relevant.

Detection of START and STOP conditions by devices connected to the bus is easy if they incorporate the necessary interfacing hardware. However, microcontrollers with no such interface has to

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sample the SDA line at least twice per clock period to sense the transition."

As described above, the I2C Spec discusses a transition on a single data line from a high voltage to a low voltage or from a low voltage to a high voltage when a clock is set high to signify the starting and stopping of data transmission over the database. The I2C Spec does not disclose forcing a number of outputs of a distribution controller to a source voltage to a common voltage in response to a start-up condition.

Such control of the voltage outputs of the distribution controller in response to a power-up condition ensures that those serial devices that are not coupled directly to the serial bus (SDA) by the bus distribution circuit are placed in a state where they will wait for further action. Otherwise, such devices might find themselves in an unwanted state after power-up and they might become confused and freeze the system or take other inadvertent action.

Accordingly, Applicant asserts that the cited combination of Simpson and the I2C Spec fails to show or suggest each of the elements of claim 1 as amended. Similarly, Applicant asserts that such cited combination fails to show or suggest the elements of claim 15 as amended to the extent that claim 15 includes subject matter similar in scope with that of claim 1. Also, Applicant notes that independent claim 10 includes subject matter that is similar in scope with that of claim 1 as amended. Accordingly, Applicant requests that the rejection of claim 10 be withdrawn for the foregoing reasons. In addition, Applicant requests that claims 1 and 15 be allowed as incorporating the subject matter of claims 4 and claims 17-18, respectively, for the above reasons. Additionally, Applicant requests that the rejection of claims 2, 11-14, and 16 be withdrawn as depending from claims 1, 10, or 15 respectively.

In addition, claim 9 has been amended so as to appear in independent form, incorporating all elements of any base claims and any intermediate claims from which claim 9 depended. In this respect, claim 9 states as follows:

9. A serial bus expansion circuit, comprising:
 - a bus distribution circuit selectively coupling a serial bus to one of a number of serial bus outputs;
 - a distribution controller having a control output coupled to a control input of the bus distribution circuit;
 - a number of power-up pull resistors coupling each of the serial bus outputs to a power-up pull source;

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a serial bus input in the distribution controller configured for coupling to the serial bus;

state circuitry in the distribution controller, the state circuitry generating a control signal that is applied to the control input of the bus distribution circuit in response to a selection message received via the serial bus, the selection message being addressed to the distribution controller; and

wherein the state circuitry applies the control signal to the control input of the bus distribution circuit upon an occurrence of an acknowledge bit in the selection message.

In this respect, claim 9 as originally filed and as amended herein recites state circuitry that applies the control signal to the control input of the bus distribution of the bus circuit upon occurrence of an acknowledge bit in the selection message. In this respect, the control signal is thus applied to the bus distribution circuit during the occurrence of the acknowledge bit thereby causing the distribution circuit to switch from a first one of the serial devices to a second one of the serial devices. This is possible because the serial devices that originally are not coupled to the serial bus SDA through the bus distribution circuit at start up are waiting to receive data due to the application of the source voltage and the ground voltage through the power-up pull resistors.

With respect to claim 9, the Office Action states:

"As to claim 9, the argument above for claim 1 applies. However, Simpson does not explicitly disclose an acknowledge bit in the selection message wherein the state circuitry applies the control signal to the control input of the bus distribution circuit upon an occurrence of the acknowledge bit. I2C Spec teaches acknowledge bit (at least 7.1-2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an acknowledge bit in the selection message wherein the state circuitry applies the control signal to the control input of the bus distribution circuit upon an occurrence of the acknowledge bit as taught by I2C Spec in the system of Simpson to let the receiver to transmit an acknowledgement and thus ensure that the transferred data has been received by the receiver and the control has been applied to the bus distribution circuit concurrently (Section 7.2)."

Applicant respectfully disagrees. Specifically, at Sections 7.1-2, the I2C Specification states:

"7 TRANSFERRING DATA

7.1 Byte format

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Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see Fig. 6). If a slave can't receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

In some cases, it's permitted to use a different format from the I²C-bus format (for CBUS compatible devices for example). A message which starts with such an address can be terminated by generation of a STOP condition, even during the transmission of a byte. In this case, no acknowledge is generated (see Section 10.1.3).

7.2 Acknowledge

Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse.

The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse (see Fig. 7). Of course, set-up and hold times (specified in Section 15) must also be taken into account.

Usually, a receiver which has been addressed is obliged to generate an acknowledge after each byte has been received, except when the message starts with a CBUS address (see Section 10.1.3).

When a slave doesn't acknowledge the slave address (for example, it's unable to receive or transmit because it's performing some real-time function), the data line must be left HIGH by the slave. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

If a slave-receiver does acknowledge the slave address but, some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not-acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates a STOP or a repeated START condition.

If a master-receiver is involved in a transfer, it must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a STOP or repeated START condition."

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As described above, the I2C Spec provides for an acknowledge bit between the bytes transmitted between devices on the serial bus. However, Applicant asserts that it is not obvious to one skilled in the art at the time of the invention to include an acknowledge bit in the selection message, where the state circuitry applies the control signal to the control input of the bus distribution current circuit upon the occurrence of the acknowledge bit. Specifically, when the control signal is applied to the control input of the bus distribution circuit, the serial bus SDA is switched from a first one of the serial devices to a second one of the serial devices. When the selection of the serial devices occurs in such manner, it is not possible for a serial device involved in the switching to transmit an acknowledgment. This is because the conductive pathway between the respective switched serial devices and the transmitting device (i.e. master device) is interrupted by the switching performed by the bus distribution circuit. Consequently, the bus distribution circuit 109 generates and transmits an acknowledgement to the transmitting (i.e. master) device. At the same time, the bus distribution circuit 109 switches the serial bus SDA from a first one of the serial devices to a second one of the serial devices.

Thus, the statement in the Office Action that "the acknowledge bit is taught by I2C Spec in the system of Simpson to let the receiver to transmit an acknowledgement and thus ensure that the transferred data has been received by the receiver and the control has been applied to the bus distribution system concurrently" makes no sense. There is no acknowledgement concurrently with the application of the control signal to the bus distribution circuit as described above.

The switching of the serial bus SDA from a first to a second one of the serial devices during the acknowledge bit provides distinct advantages. Specifically, since the clock SCL is low during the acknowledge bit, the switch between serial devices may take place without confusing the serial devices. This is because, at power up, the serial devices are placed in a state where they are waiting to receive data as set forth in claim 9. By switching during an acknowledge bit or other point in the transmission where the clock SCL is held low, the device to which the serial bus SDA is switched receives the data without detecting a start or stop condition, or becoming confused in some other manner. This provides an advantage in that switching between serial devices is accomplished with greater speed and without interrupting the operation of the devices communicating on the serial bus to place them in an idle state to facilitate switching.

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Accordingly, Applicant asserts that claim 9 is improper. Therefore, Applicant requests that the rejection of claim 9 be withdrawn. In addition, Applicant notes that claim 19 has been amended herein so as to appear in independent form. Applicant requests that the rejection of claim 19 be withdrawn to the extent that claim 19 incorporates subject matter similar in scope with that of claim 9.

CONCLUSION

Applicants respectfully request that all outstanding objections and rejections be withdrawn and that this application and all presently pending claims be allowed to issue. If the Examiner has any questions or comments regarding Applicants' response, the Examiner is encouraged to telephone Applicants' undersigned counsel.

Respectfully submitted,



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